CLAIMS:

1. A system for broadcasting multi-channel signals to a receiving station over a two-wire bus, comprising:

an encoder having:

a multiplexer for multiplexing digital data corresponding to the channel signals and producing a data stream;

a framer connected to the multiplexer, for breaking the data stream up into frames, and for inserting into said frame a header containing at least a predetermined pattern;

a transceiver with pre-emphasis connected to the framer of the encoder and connectable to the two-wire bus;

a receiver with de-emphasis, connectable to the two-wire bus, said receiver including:

a decoder connectable to the receiving station, the decoder having a de-framer for reproducing the digital data corresponding to selected ones of the multi-channel signals from the frames, said de-framer being adapted to use a previous frame when an error condition is detected in a current frame;

a synchronization circuit using a pattern-oriented phase-locked loop for sampling the incoming data stream using said predetermined pattern, and for regenerating a system clock; and

a channel selector circuit connected to the de-framer and controlling which ones of the multi-channel signals are reproduced by the de-framer.

2. The system according to claim 1, wherein:

the encoder has delta-sigma analog-to-digital converters for converting the multi-channel signals into digital form for the multiplexer; and

the decoder has a delta-sigma digital-to-analog converter connected to the de-framer for converting the digital data corresponding to the selected ones of the multi-channel signals into analog form for the receiving station.

3. The system according to claim 2, wherein the encoder comprises analog interfaces respectively having amplifiers in series with low pass filters for amplifying and filtering the multi-channel signals transmitted to the delta-sigma analog-to-digital converters.

4. The system according to claim 1, wherein:

the encoder comprises a compression circuit for compressing the digital data input into the framer; and

the decoder comprises a decompression circuit for decompressing the digital data output by the de-framer.

5. The system according to claim 4, wherein the compression circuit and the decompression circuit have look-up tables defining compression and decompression functions respectively.

6. The system according to claim 4, wherein the compression circuit and the decompression circuit respectively have logarithmic and antilogarithmic functions.

7. The system according to claim 1, wherein the multiplexer has a time division multiplexing function.

8. The system according to claim 1, wherein said header has less transitions than transitions in the digital data.

9. The system according to claim 8, wherein the header has a size of 17 bits.

10. The system according to claim 1, wherein the frames comprise a parity bit for data integrity check by the decoder.

11. The system according to claim 1, wherein the synchronization circuit comprises a sampling circuit for sampling the frames in at a number of times an

incoming data rate, a test circuit for testing a phase relation of the frames with an internal reference, and a phase lock loop circuit responsive to the test circuit for phase correction of the synchronization circuit.

12. The system according to claim 12, wherein the test circuit is adapted to perform a phase comparison after finding a predetermined bit pattern in the data stream.

13. The system according to claim 1, wherein the channel selector circuit comprises a user interface for selection of said ones of the multi-channel signals.

14. The system according to claim 1, wherein the decoder has a variable gain amplifier for amplifying the selected ones of the multi-channel signals, and a user interface for adjusting a gain of the variable gain amplifier.

15. The system according to claim 1, wherein the de-framer comprises a synchronization analyzer receiving a signal indicative of the selected ones of the multi-channel signals, and serial to parallel converting circuitry controlled by the analyzer for providing the digital data into parallel form.

16. The system according to claim 1, further comprising a data repeater connectable between the two-wire bus and an additional two-wire bus, for rebuilding, cleaning up and repeating the frames for transmission on the additional two-wire bus.

17. The system according to claim 16, wherein:

the data repeater comprises a sampler for sampling the frames in at a number of times an incoming data rate, a test circuit for testing a phase relation with an internal reference, a feedback circuit responsive to the test circuit for correction of the internal reference used by the sampler and the test circuit, and a correction circuit for phase correction of the frames going out from the repeater; and

the system further comprising a transceiver with pre-emphasis connected to the data repeater and connectable to the additional two-wire bus.

18. The system according to claim 17, wherein the data repeater has a phase locked on one clean pulse intentionally generated by the encoder, the frames being sampled by the sampler based on the phase.

19. The system according to claim 17, wherein the correction circuit comprises a digital filter.

10

20. The system according to claim 17, wherein the number of times is higher than a number of times the frames are sampled by the decoder.

21. The system according to claim 1, wherein the multi-channel signals comprise multiple channels of audio stereo signals, and the receiving station comprises an audio listening station.

22. The system according to claim 1, wherein the multi-channel signals comprise high speed applications.

20

23. The system according to claim 2, wherein the decoder has at least one additional delta-sigma digital-to-analog converter connected to the de-framer, for converting the digital data corresponding to additional selected ones of the multi-channel signals.

24. The system according to claim 1, wherein the receiver has outputs for connection to the decoder and to additional like decoders.

25. The system according to claim 1, wherein the two-wire bus forms a

30 serial multi-drop communication network.

26. A method of broadcasting high-speed applications over a serial multi-drop communication network, comprising:

time-division multiplexing the high-speed applications to produce a data stream;

framing the data stream into frames having a header and a parity bit, the header having a size lower than 32 bits;

transmitting the frames with pre-emphasis over the serial multi-drop communication network;

receiving the frames with de-emphasis from the serial multi-drop communication network;

detecting a predetermined bit pattern in the received frames;

synchronizing the received frames using an internal clock signal and an external clock signal found within the frames following a phase comparison made after detection of the predetermined bit pattern; and

de-framing the synchronized frames into a selected one of the high-speed applications.

27. The method according to claim 26, further comprising analog-to-digital converting the high-speed applications prior to the multiplexing, and digital-to-analog converting the selected one of the high-speed applications after the de-framing.

28. The method according to claim 27, wherein the analog-to-digital converting and the digital-to-analog converting comprise over sampling and closed-loop modulating the high-speed applications.

29. The method according to claim 26, wherein the high-speed applications comprise a multi-channel signal broadcast.

30. The method according to claim 26, further comprising parallel to series converting the high-speed applications prior to the multiplexing, and series to parallel converting the selected one of the high-speed applications.

31. The method according to claim 26, further comprising checking data integrity of the synchronized frames using the parity bit.

32. The method according to claim 31, wherein a previously received frame is used when an error condition is detected in a currently received frame.

33. The method according to claim 26, wherein the high-speed applications comprise a multi-channel audio signal broadcast to audio listening stations connected to the serial multi-drop communication network.

34. The method according to claim 26, wherein the predetermined bit pattern is located in the header of the frames.

35. The method according to claim 26, further comprising compressing the high-speed applications prior to the framing, and decompressing the selected one of the high-speed applications after the de-framing.

36. The method according to claim 26, further comprising repeating the frames for transmission over another segment of the serial multi-drop communication network.

37. The method according to claim 26, wherein the repeating comprises sampling the frames in at a number of times an incoming data rate, testing a phase relation with an internal reference, phase correcting the frames going out to the other segment, and transmitting the frames with pre-emphasis to the other segment.

38. The method according to claim 37, further comprising inserting a clean pulse in the frames, and locking a phase on the clean pulse for sampling the frames.

39. The method according to claim 37, wherein the number of times is higher than a number of times the frames are sampled in the synchronizing.